REMARKS

The present Amendment forwards a replacement drawing that designates Figure 1 as prior art, as required in Section 1 of the Office Action.

The present Amendment also provides a title that is more descriptive, as required in Section 2 of the Office Action. The new title is "SEMICONDUCTOR CIRCUIT WITH FLASH ROM AND IMPROVED SECURITY FOR THE CONTENTS THEREOF."

In addition, the present Amendment revises the specification and abstract to improve the idiomatic English and correct inadvertent informalities.

Furthermore, the present Amendment revises all of the claims in order to improve their form under U.S. claim-drafting practice, and also in order both delete unnecessary limitations and further distinguish the invention. As part of the claim revisions, claims 2 and 3 have been changed from independent claims to claims that depend from claim 1. It is respectfully submitted that the claims, as revised, are now suitably definite under the second paragraph of 35 USC §112. Accordingly, the rejections in Sections 4 and 5 of the Office Action should be withdrawn.

The present application discloses several embodiments of a technique for keeping the contents of a flash memory from being read out by an unauthorized third party. This is accomplished by using a security bit that is read out of the flash memory to control whether or not communication of signals between a JTAG (Joint Test Action Group) port and a TAP (Test Access Port) will be permitted or not.

Section 7 of the Office Action rejects claims 1 and 4 - 8 for anticipation by Iwata et al. (hereafter simply "Iwata"). For the reasons discussed below, however, it is respectfully submitted that the invention now defined by the independent claims is patentable over this reference.

The Iwata reference discloses a microcomputer with flash memory 5 having an internal circuit 5c which controls whether rewriting will be prohibited or allowed. To this end, a mode signal and a flash-protect signal are supplied to OR gate 5b, whose output is received by the internal control circuit 5c.

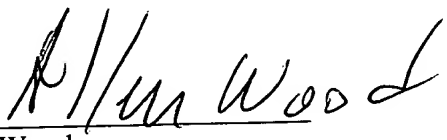
Independent claim 1 now recites "a JTAG control circuit controlled by the security bit of the flash ROM, the JTAG circuit being connected between the JTAG port and the TAP and allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit." The Iwata reference neither discloses nor suggests such a JTAG control circuit.

Independent claim 4 recites "a unit to control on/off between the test port and at least one of the memory device and the central processing unit according to the security bit set in the nonvolatile register ...". Independent claim 8 recites "a switch to control on/off between the test port and the central processing unit" and "a security releasing means for comparing data input via the test port with the data stored in the memory device and turning on the switch when the two data agree." These features, it is respectfully submitted, are neither disclosed nor suggested by Iwata.

Since claims 5 - 7 depend from claim 4 and recite additional limitations to further define the invention, they are patentable along with claim 4 and need not be further discussed.

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



Allen Wood
Registration No. 28,134
RABIN & BERDO, PC
Customer No. 23995
Telephone: 202-371-8976
Facsimile: 202-408-0924

AW:pjl/rw